

Abstract of the Disclosure

A FOS circuit and a method for fabricating the same that reduces the possibilities of shorts or damage to a circuit board during assembly due to solder reflow. The FOS circuit has a tail, a shunt bar, a plurality of flying leads, and a dam. The tail has a first and second end. The shunt bar is located adjacent to the second end of the tail. The plurality of flying leads project substantially perpendicular from the first edge of the second end of the tail. The plurality of flying leads are substantially parallel to one another and extend between the second end of the tail and the shunt bar. A plurality of electrical paths are formed through the tail to the flying leads. The dam intersects the flying leads and extends from a first flying lead to a last flying lead and is substantially parallel with the first edge of the second end of the tail.

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